IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims, AMEND claims, and ADD new claims, in accordance with the following:

1. (ORIGINAL) An error detection/correction system in data transmission between a plurality of modules that are connected via buses in a controller, wherein

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the system, and

an the error detection/correction code generation circuit and the error detection/correction circuit to be used are switched over dependent upon a kind, a length, and a timing of the data to be transferred.

2. (ORIGINAL) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over between error detection/correction codes to be used dependent upon on a phase of transmitting an address, a command, and data.

3. (ORIGINAL) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over error detection/correction codes to be used dependent upon whether at a time of single access or at a time of burst access.

4. (ORIGINAL) The error detection/correction system according to claim 1, wherein the error detection/correction system switches over between error detection/correction codes to be used, dependent upon a data quantity to be transferred.

5. (CURRENTLY AMENDED) A controller in which a plurality of modules that adopt the error detection/correction system according to ~~any one of claims 1 to 4~~ claim 1 are

connected via buses.

6. (CURRENTLY AMENDED) The controller according to claim 5, wherein

the controller comprises a serial transfer module that connects a plurality buses connected with the plurality of modules, by means of a serial transmission line, and

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the serial transfer module, and the error detection/correction system according to ~~any one of claims 1 to 4~~ claim 1 is used also for the serial transfer.

7. (NEW) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 2 are connected via buses.

8. (NEW) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 3 are connected via buses.

9. (NEW) A controller in which a plurality of modules that adopt the error detection/correction system according to claim 4 are connected via buses.

10. (NEW) The controller according to claim 5, wherein

the controller comprises a serial transfer module that connects a plurality buses connected with the plurality of modules, by means of a serial transmission line, and

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the serial transfer module, and the error detection/correction system according to claim 2 is used also for the serial transfer.

11. (NEW) The controller according to claim 5, wherein

the controller comprises a serial transfer module that connects a plurality buses connected with the plurality of modules, by means of a serial transmission line, and

a plurality of error detection/correction code generation circuits having a difference in at

least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the serial transfer module, and the error detection/correction system according to claim 3 is used also for the serial transfer.

12. (NEW) The controller according to claim 5, wherein

the controller comprises a serial transfer module that connects a plurality buses connected with the plurality of modules, by means of a serial transmission line, and

a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and error detection/correction circuits corresponding to the error detection/correction code generation circuits are built into the serial transfer module, and the error detection/correction system according to claim 4 is used also for the serial transfer.